Shallow Trench Isolation

- Clean
- Grow pad oxide
- Deposit silicon nitride (1)
- Clean
- Prep/spin-on photoresist/soft bake
- STI mask alignment and exposure (2)
- Postexposure bake/develop/hard bake
- Pattern inspection
- Etch nitride/pad oxide
- Strip photoresist
- Clean
- Etch silicon (3)
- Clean
- Grow barrier oxide
- HDP-CVD USG (4)
- CMP USG (5)
- Anneal USG
- Wet strip nitride and pad oxide (6)

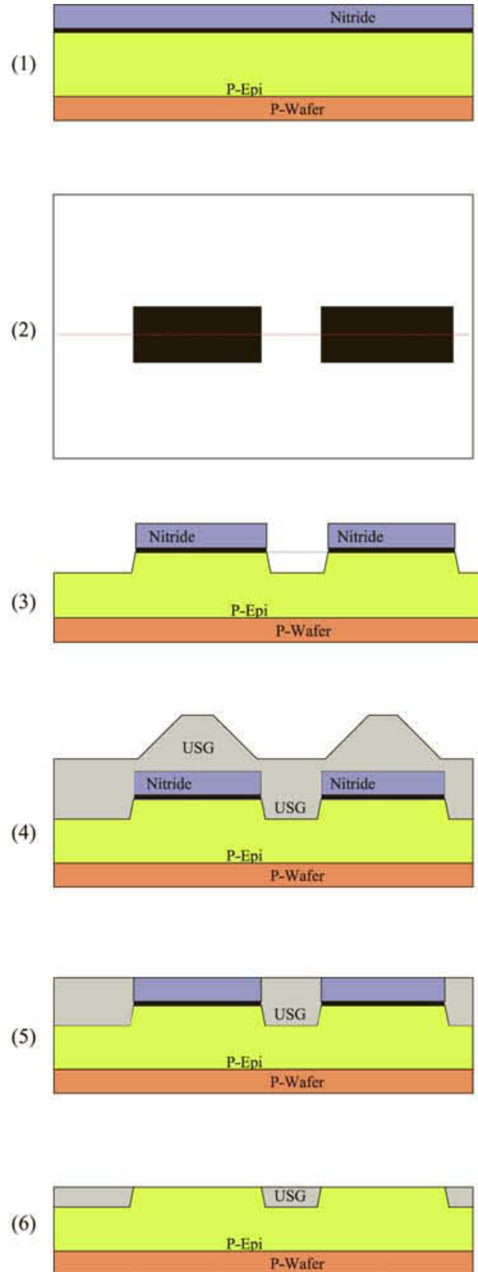


Figure 14.4 CMOS process with multilayer Al alloy interconnects (*continued on following 11 pages*).

Well Formation

•Clean

•Grow screen oxide

•Clean

•Prep/spin-on phtoresist/soft bake

•n-well mask alignment and exposure (7)

•Postexposure bake/develop/hard bake

•Inspection

•n-well ion implantation, phosphorus (8)

•Strip photoresist

•Clean

•Anneal and drive-in

•Clean

•Prep/spin-on photoresist/soft bake

•p-well mask alignment and exposure (9)

•Postexposure bake/develop/hard bake

•Inspection

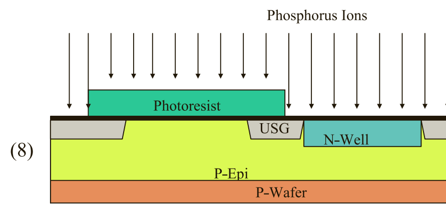
•p-well ion implantation, boron (10)

•Strip photoresist

•Anneal and drive-in (11)

(7)

(8)



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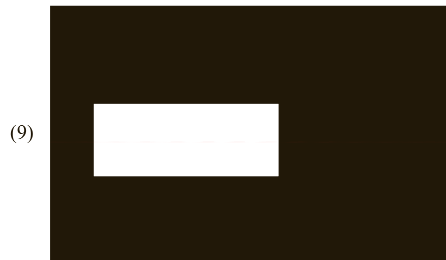

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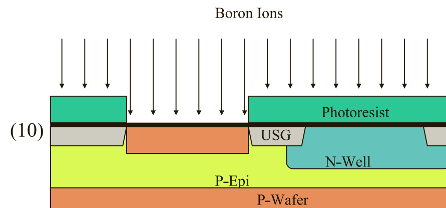

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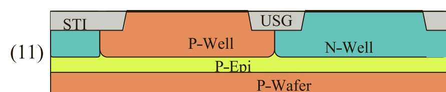
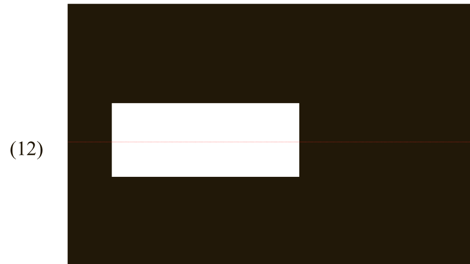


Figure 14.4 (*continued*)

- Clean
- Grow sacrificial oxide
- Clean
- Prep/spin-on photoresist/soft bake
- n-channel V_T mask alignment and exposure (12)
- Postexposure bake/develop/hard bake
- Pattern inspection
- n-channel V_T adjust implantation (13)
- Strip photoresist
- Clean
- Prep/spin-on photoresist/soft bake
- p-channel V_T mask alignment and exposure (14)
- Postexposure bake/develop/hard bake
- Pattern inspection
- p-channel V_T adjust implantation (15)
- Strip photoresist/clean
- Rapid thermal annealing (16)
- Strip sacrificial oxide

(12)



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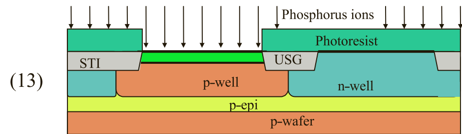

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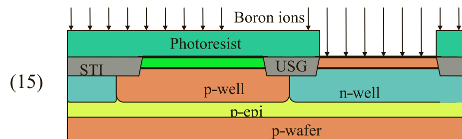

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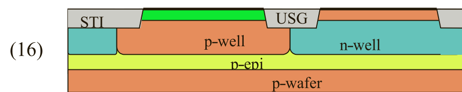

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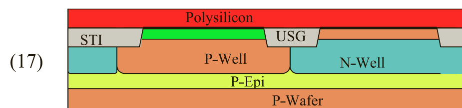
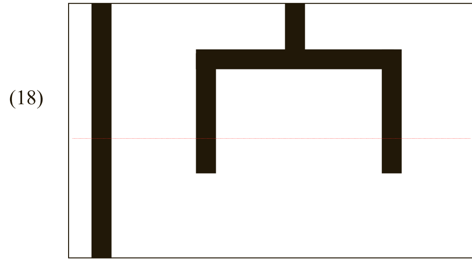


Figure 14.4 (*continued*)

- •Clean
- •Strip native oxide
- •Grow gate oxide
- •Deposit polysilicon (17)
- •Clean
- •Prep/spin-on photoresist/soft bake
- •Gate mask alignment and exposure (18)
- •Postexposure bake/develop/hard bake
- •Inspection
- •Etch polysilicon (19)
- •Strip photoresist
- •Clean
- •Polysilicon anneal/oxidation
- •Clean
- •Prep/spin-on photoresist/soft bake
- •n-channel LDD mask (20)
- •Postexposure bake/develop/hard bake
- •Inspection
- •n-channel LDD implantation (21)
- •Strip photoresist
- •Clean
- •Prep/spin-on photoresist/soft bake

(18)



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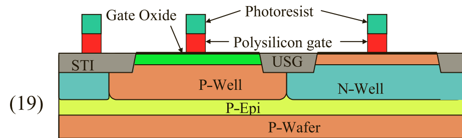

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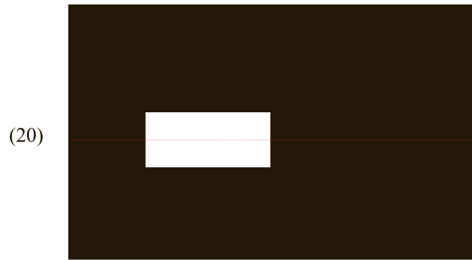

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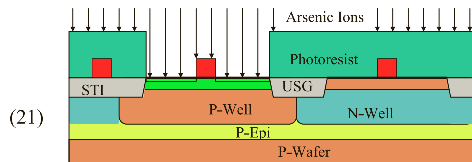

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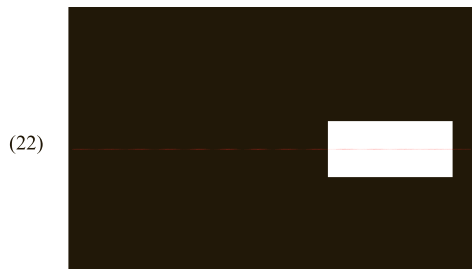
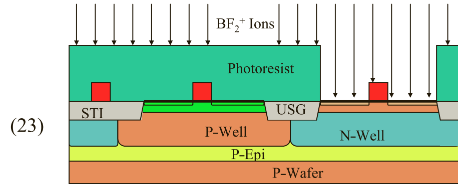


Figure 14.4 (*continued*)

- •p-channel LDD mask (22)
- •Postexposure bake/develop/hard bake
- •Pattern inspection
- •p-channel LDD implantation (23)
- •Strip photoresist
- •Clean
- •LPCVD nitride
- •CVD O_3-TEOS USG (24a)
- •USG etchback, stop on nitride (24b)
- •Clean
- •Prep/spin-on photoresist/soft bake
- •n-channel S/D mask (25)
- •Postexposure bake/develop/hard bake
- •Inspection
- •n-channel S/D implantation (26)
- •Strip photoresist
- •Clean
- •Rapid thermal annealing
- •Clean
- •Prep/spin-on photoresist/soft bake
- •p-channel S/D mask (27)
- •Postexposure bake/develop/hard bake

(23)



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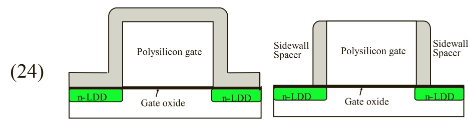

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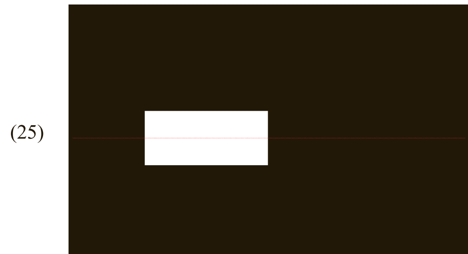

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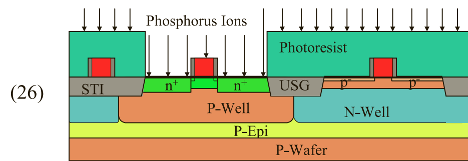
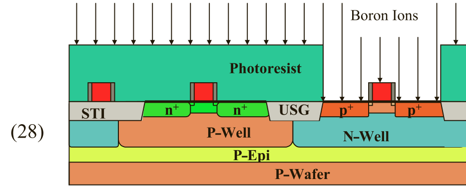


(27)

Figure 14.4 (*continued*)

- Inspection
- p-channel S/D implantation (28)

(28)

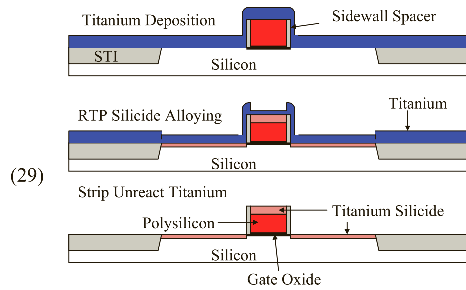


- Strip photoresist
- Clean
- Rapid thermal annealing

<u>Global Interconnection</u>

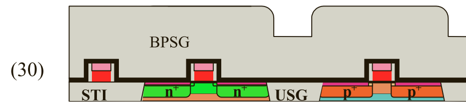
- Degas
- Argon sputtering preclean
- Sputtering deposit titanium (29a)
- Rapid thermal anneal (29b)
- Wet strip titanium (29c)

(29)



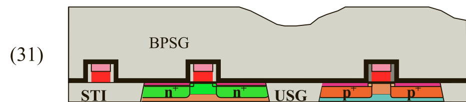
- Second silicide annealing
- Deposit nitride
- O_3-TEOS based BPSG CVD (30)

(30)



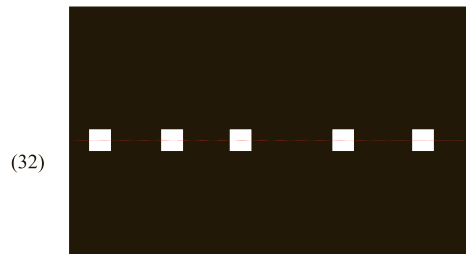
- Reflow of BPSG (31)

(31)



- BPSG CMP
- Clean
- Prep/spin-on photoresist/soft bake
- Contact mask (32)

(32)



- Postexposure bake/develop/hard bake
- Inspection

Figure 14.4 (*continued*)

•Etch BPSG, Stop on silicide surface

•Strip photoresist (33)

•Clean

•Degas

•Argon sputtering pre-PDV clean

•Deposit Ti/TiN by both PVD and CVD

•CVD tungsten (34)

•Polish tungsten/TiN/Ti

•Clean

• Ar sputtering pre-PDV clean

•PVD Ti

•PVD of Al-Cu alloy

•PVD of TiN ARC layer (35)

•Clean

•Prep/spin-on photoresist/soft bake

•Metal-1 mask (36)

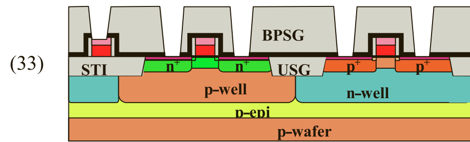
•Postexposure bake/develop/hard bake

•Inspection

•Etch metal

•Strip photoresist (37)

(33)



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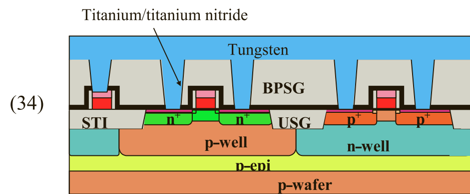

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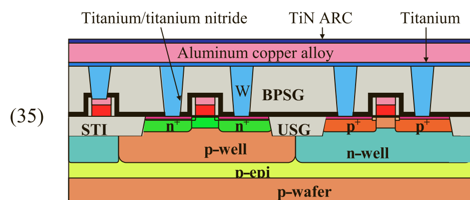


(36)

(37)

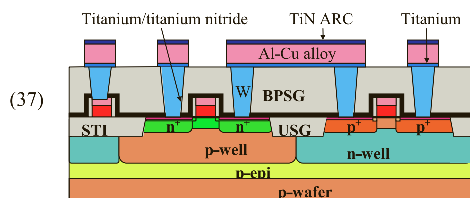
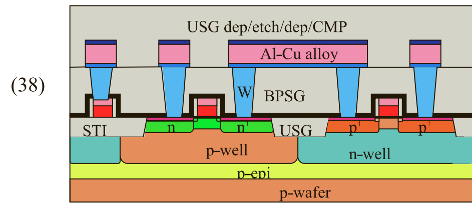


Figure 14.4 (*continued*)

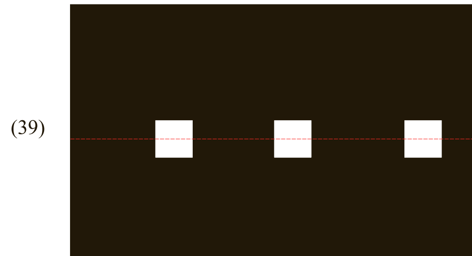
- •Metal anneal
- •CVD USG
- •Sputtering etchback USG
- •CVD USG
- •CMP USG (38)

(38)



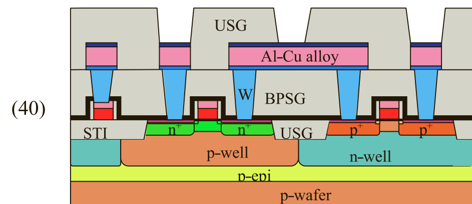
- •Clean
- •Prep/spin-on photoresist/soft bake
- •Via-1 mask (39)
- •Postexposure bake/develop/hard bake
- •Inspection

(39)



- •Etch USG
- •Strip photoresist (40)

(40)



- •Degas
- •Ar^+ sputtering preclean
- •Deposit Ti/TiN
- •Deposit tungsten
- •Polish tungsten/TiN/Ti
- •Ar^+ sputtering pre-clean
- •Deposit Ti
- •Deposit Al•Cu
- •Deposit TiN (41)

(41)

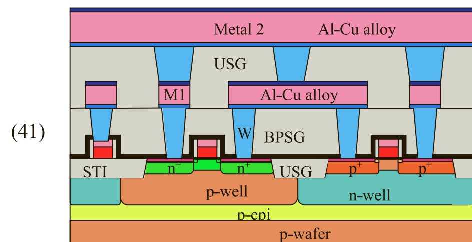
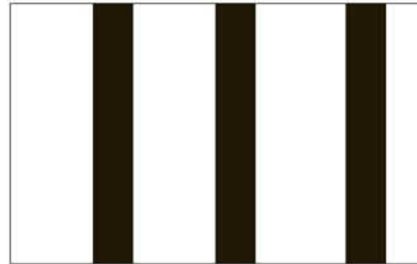


Figure 14.4 (*continued*)

- •Clean
- •Prep/spin-on photoresist/soft bake
- •Metal-2 mask (42)
- •Postexposure bake/develop/hard bake
- •Inspection
- •Etch metal 2
- •Strip photoresist/clean (43)
- •Metal annealing
- •Deposit USG, PE-TEOS
- •USG sputter etchback, Ar^+
- •CVD USG, PE-TEOS
- •CMP USG (44)
- •Prep/spin-on photoresist/soft bake
- •Via-2 mask (45)
- •Postexposure bake/develop/hard bake
- •Inspection
- •Etch USG
- •Strip photoresist (46)
- •Clean
- •Degas
- •Ar^+ sputtering preclean

(42)



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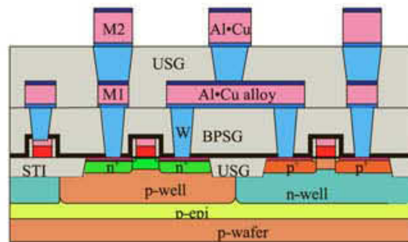

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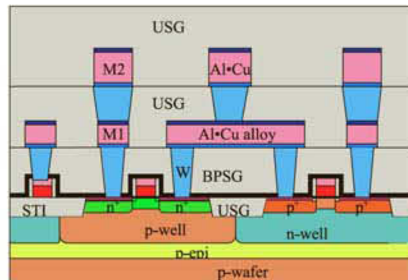

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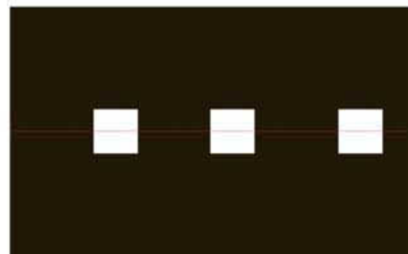
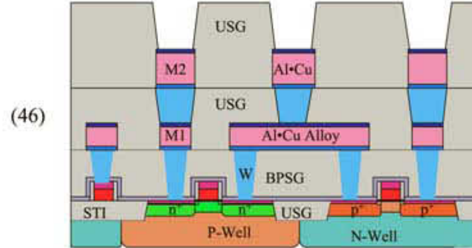


Figure 14.4 (*continued*)

- •Deposit Ti/TiN
- •Deposit tungsten
- •Polish W/TiN/Ti
- •Clean
- •Degas
- •Ar^+ sputtering preclean
- •Deposit titanium
- •Deposit Al-Cu
- •Deposit titanium nitride (47)
- •Clean
- •Prep/spin-coat photoresist/soft bake
- •Metal-3 mask (48)
- •Postexposure bake/develop/hard bake
- •Inspection
- •Etch metal 3
- •Strip photoresist (49)
- •Clean
- •Metal annealing
- •CVD USG, PE-TEOS
- •Ar sputtering etchback
- •CVD USG, PE-TEOS

(46)



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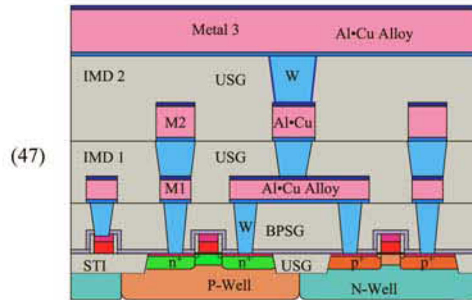

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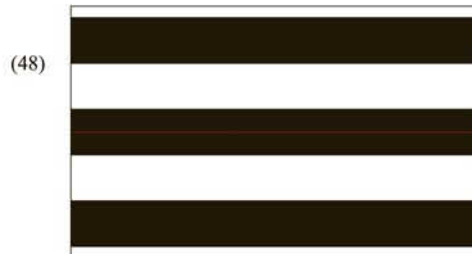

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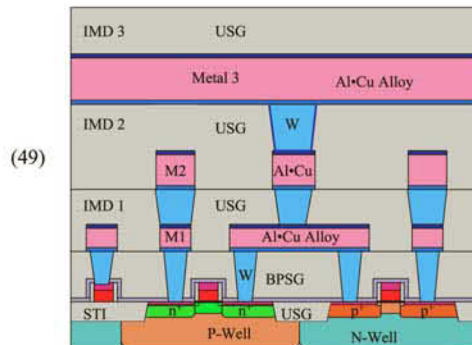
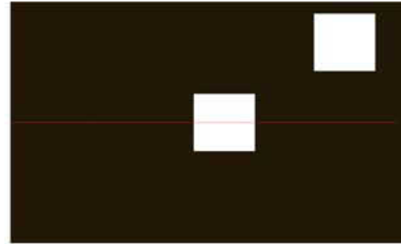


Figure 14.4 (*continued*)

Next Page

- •CMP USG
- •Clean
- •Prep/spin-coat photoresist/soft bake
- •Via-3 mask (50)
- •Postexposure bake/develop/hard bake
- •Inspection
- •Via-3 etch
- •Strip photoresist (51)
- •Clean
- •Ar sputtering preclean
- •Deposit titanium
- •Deposit Al-Cu
- •Deposit titanium nitride (52)
- •Clean/prep/spin-coat photoresist/soft bake
- •Metal-3 mask (53)
- •Postexposure bake/develop/hard bake/inspection
- •Etch metal 4
- •Strip photoresist (54)
- •Clean
- •Metal annealing

(50)



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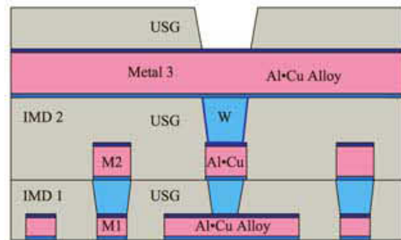

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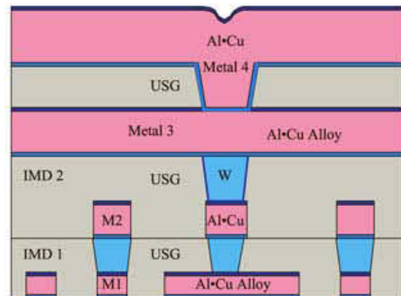

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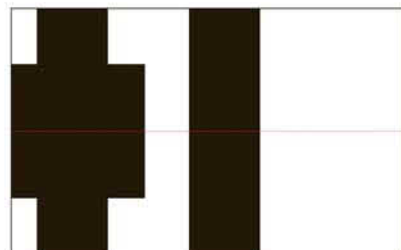

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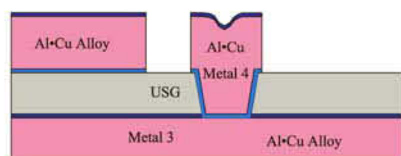

Figure 14.4 (*continued*)