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Fabrication of Metal Oxide Semiconductor

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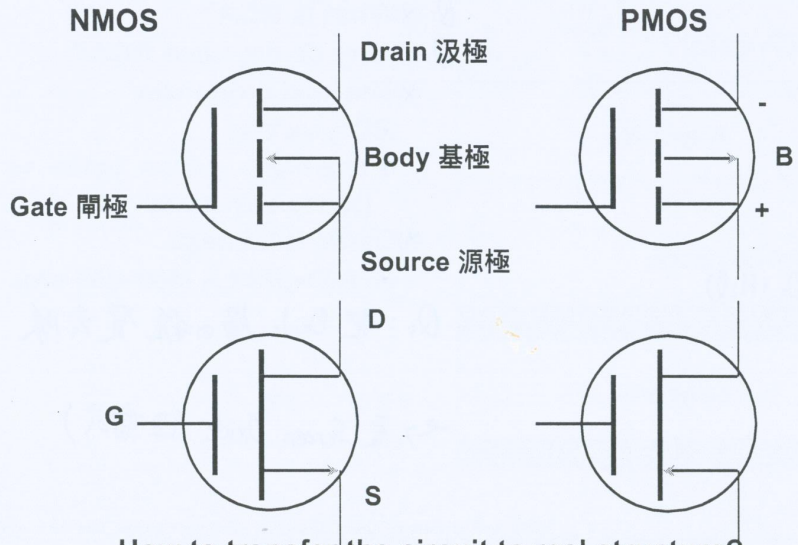
Introduction

Enhanced-MOSFET (E-MOSFET) circuit



How to transfer the circuit to real structure?

metal oxide semi-conductor

NMOS vs PMOS

圖 2 增強型N通道MOS電晶體

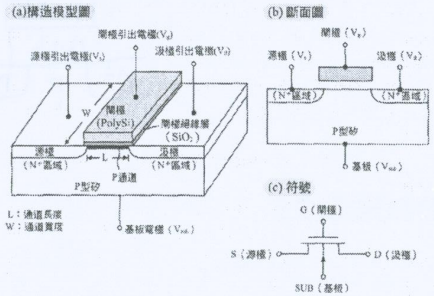


圖 3 NMOST (E) 的電流 (I) －電壓 (V) 特性與特性式

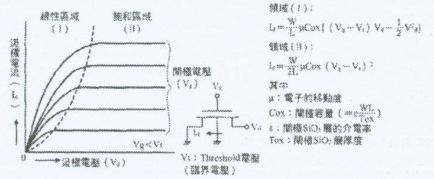
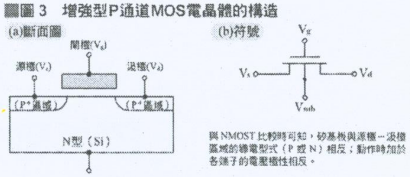
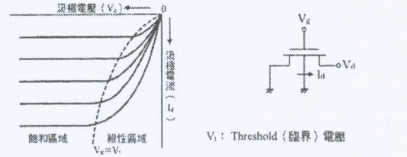


圖 3 增強型P通道MOS電晶體的構造



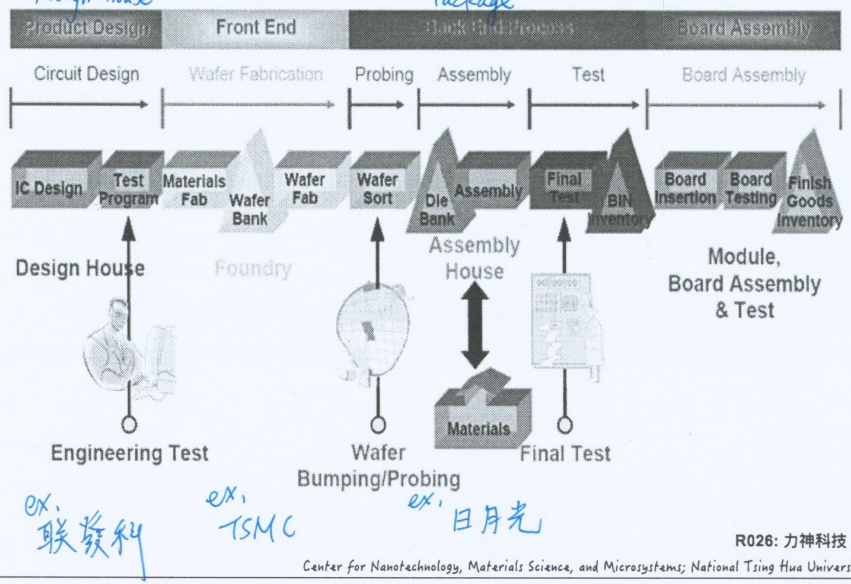
與 NMOST 比較時可知，矽基板與源極－汲極區域的導電型式（P 或 N）相反；動作時加於各端子的電壓極性相反。

圖 4 增強型P通道MOS電晶體的I－V特性



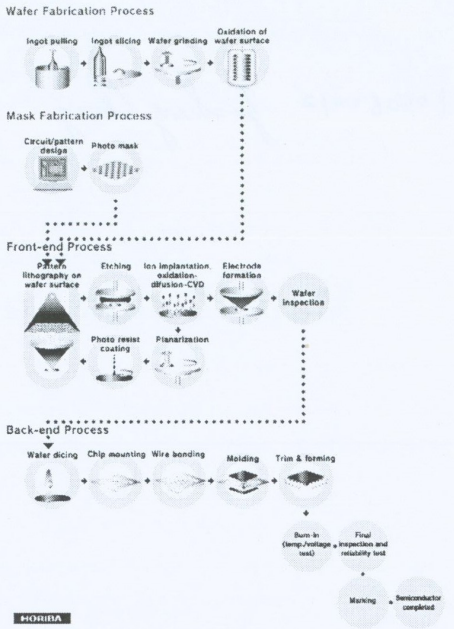
Vt：Threshold（臨界）電壓

Overview of semiconductor process - I

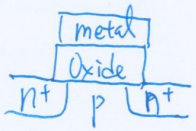


R026: 力神科技

Overview of semiconductor process - II



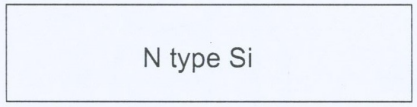
PMOS process



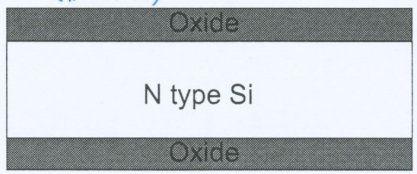
* Wet Oxidation 可以讓 Oxide 長得較厚，以利阻擋(BOE) Wet Etching

Oxidation

1. RCA clean



2. Wet Oxidation ($O_2 + H_2O$)



- Q1 ⊗What is RCA?
- Q2 ⊗Why do we need RCA?
- ⊗Thermal oxidation
  - ⊙Dry vs Wet
  - ⊙Thermally grown oxide vs Deposition oxide
- ⊗Oxide thickness
  - ⊙4000~5000 Å (400~500 nm)

Q1：把 Oxide 層的雜質去除

↪ 長 Screen Oxide (阻擋層)

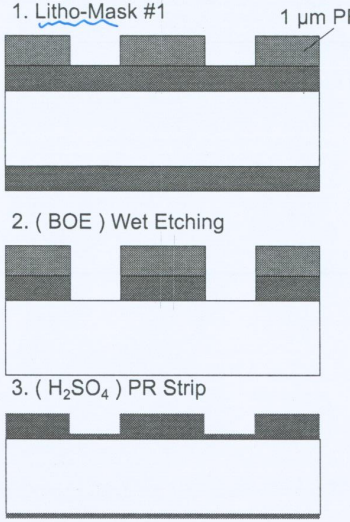
RCA clean

- Preliminary Cleaning (SPM)
  - Organic contamination is removed with a 5:1 H_2SO_4:H_2O_2 solution at 120℃.
- Standard clean-1 (SC-1)
  - Removal of insoluble organic contaminants/ particles with a 5:1:1 H_2O(DI water):H_2O_2:NH_4OH solution at 75℃.
  - Particles: Group IB, IIB, Au, Ag, Cu, Ni, Zn, Cd, Co, and Cr.
- Standard clean-2 (SC-2)
  - Removal of ionic and heavy metal atomic contaminants using a 75℃ solution of 6:1:1 H_2O:H_2O_2:HCl.
  - Metal: alkali ions and cations like Al^{+3}, Fe^{+3}, Mg^{+2}, (Au).
- Oxide strip
  - Removal of a thin silicon dioxide layer where metallic contaminants may accumulated as a result of cleaning, using a diluted 50:1/ 10:1 H_2O:HF solution.

↳ 氫氟酸, 化骨水

Lithography 1: Defining the source and drain

↳ use photoresistance



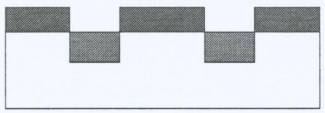
- Lithography process (微影製成)
  - Photoresist (PR) coating
  - Soft bake
  - Exposure
  - Development
  - Hard back
- Wet etching
  - BOE vs HF
- PR stripping (剝離)
  - H_2SO_4 vs Stripper

PR < positive PR (和 photo-mask 形同)
negative PR (和 photo-mask 顛倒)

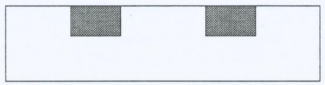
Dopant doping

* 所有的電信設計, 在 crystal 設計
* Si 在自然環境下 30min 後會變 結晶下
  成 SiO_2 (非結晶態)

1. BOE dip
2. Diffusion → Need RTA



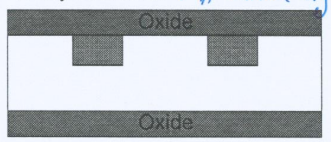
3. (BOE) Wet Etching



- Why dipping BOE first
- Dopant
  - N-dopant: Phosphor (磷)
  - P-dopant: Boron (硼)
- Ion implantation vs Thermal diffusion
  - Profile, cycle time…
- RTA (Rapidly thermal annealing) at 1000°C for 30s in Ar or N_2
  - Why RTA
  - Why no RTA for diffusion process
- Screen oxide removing

Gate oxide formation

1. Dry Oxidation (易 control signal)

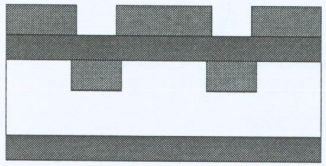


- Dry oxidation at 950°C to grow a oxide with 20-50 nm in thickness
  - Wet oxide vs Dry oxide
    - Last one is wet oxide, why don't we use wet oxide again?
  - Low temperature vs High temperature

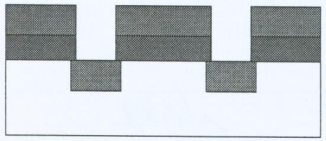
• oxide 的厚度 (t_{ox}) will affect the value of C_{ox}, which will affect drain current

Lithography 1: Defining the gate oxide

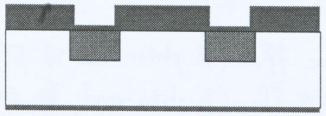
1. Litho-Mask #3



2. (BOE) Wet Etching



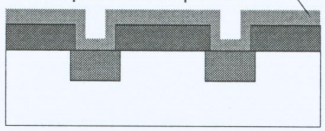
3. (H_2SO_4) PR Strip



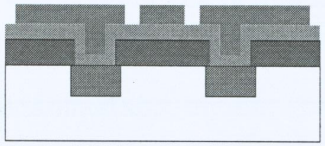
- What is alignment?
  - Size
  - Position
  - Type

Metallization

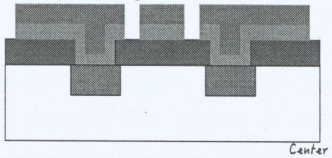
1. BOE dip
2. Evaporator or Sputter



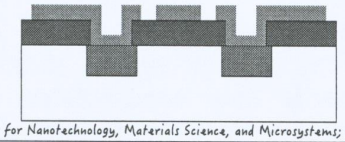
1. Litho-Mask #4



2. Dry Etching



3. (Acetone) PR Strip



- 400nm Al
  - E-gun evaporation vs Sputter
- Sulfuric acid vs Acetone
- Purpose of RTA