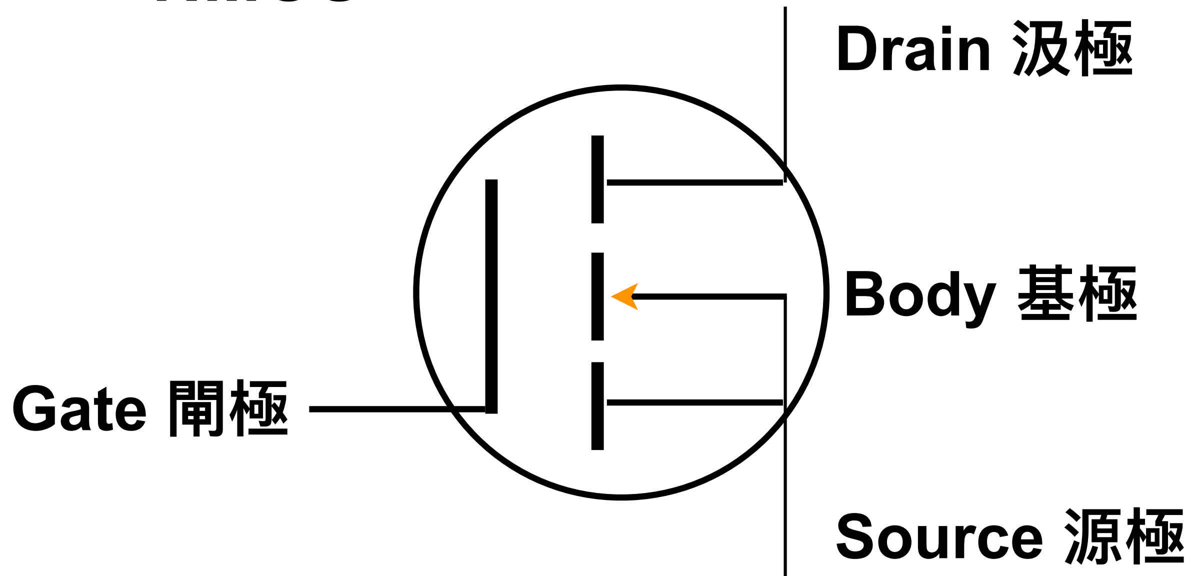
Fabrication of Metal Oxide Semiconductor

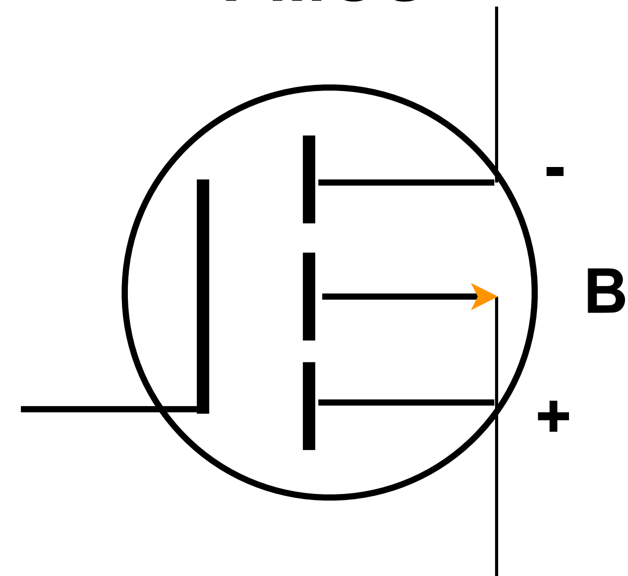
岑尚仁 博士
奈材中心 副研究員

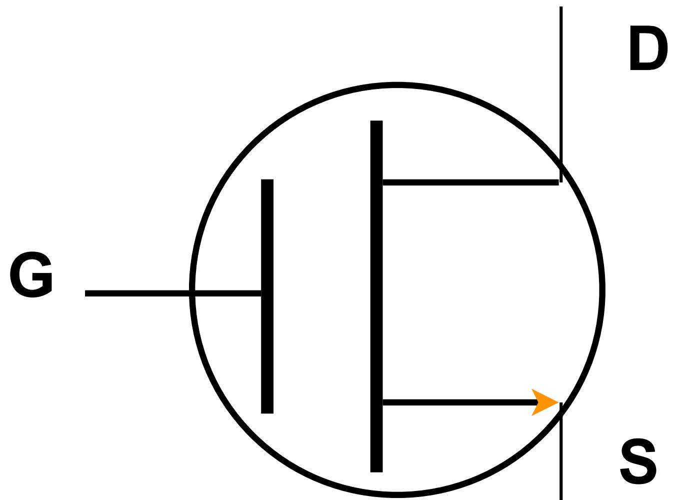
Introduction

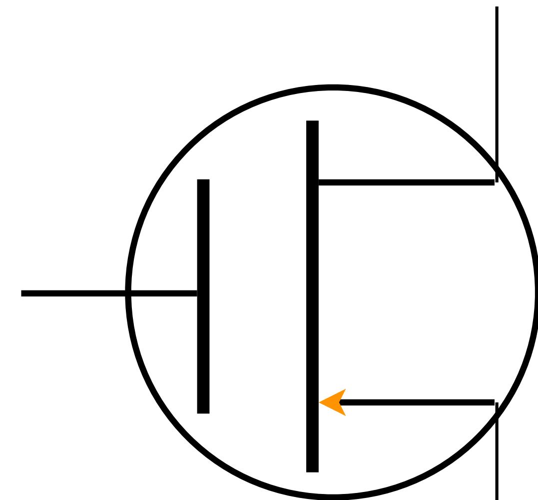
Enhanced-MOSFET (E-MOSFET) circuit

NMOS **PMOS**





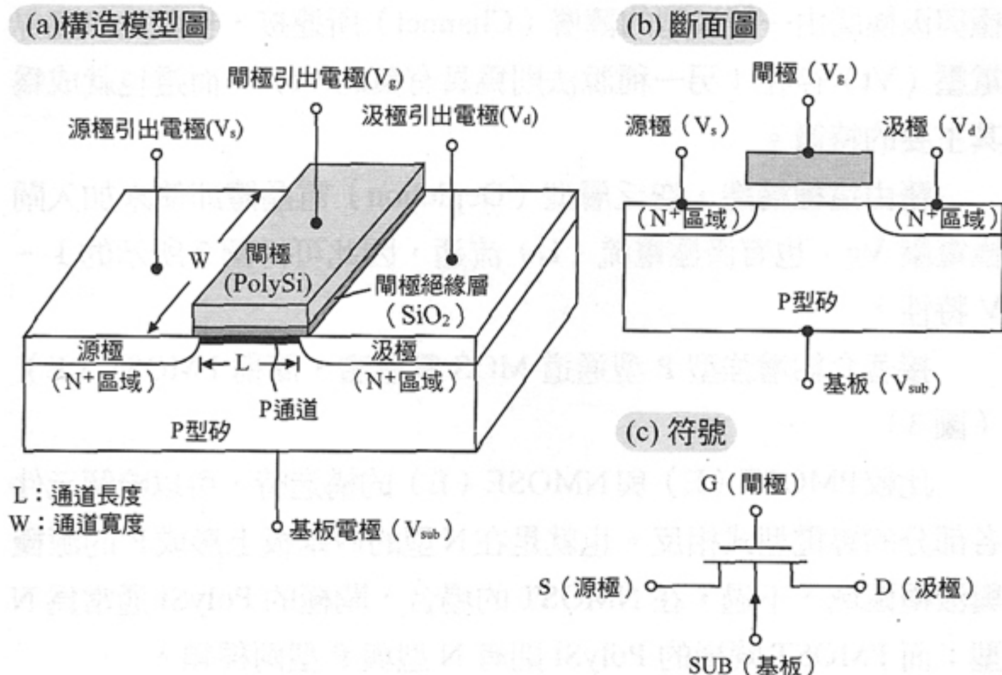




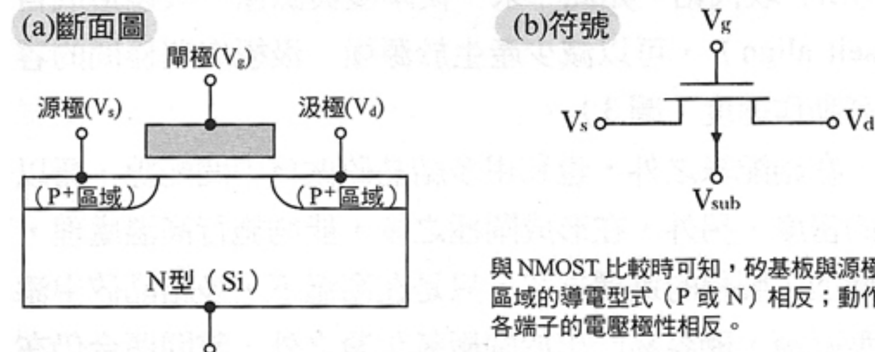
How to transfer the circuit to real structure?

NMOS vs PMOS

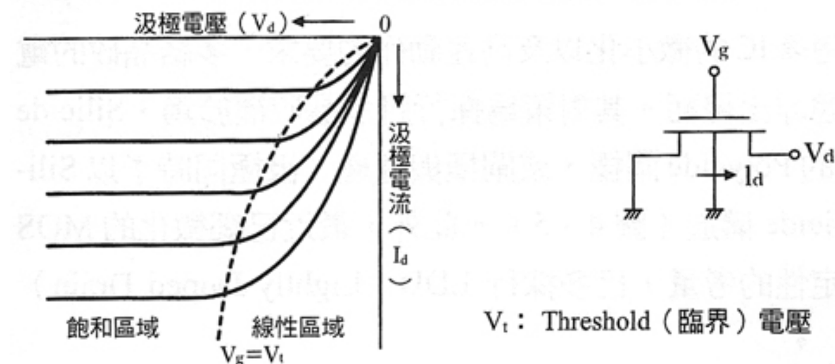
■圖 2 增強型N通道MOS電晶體



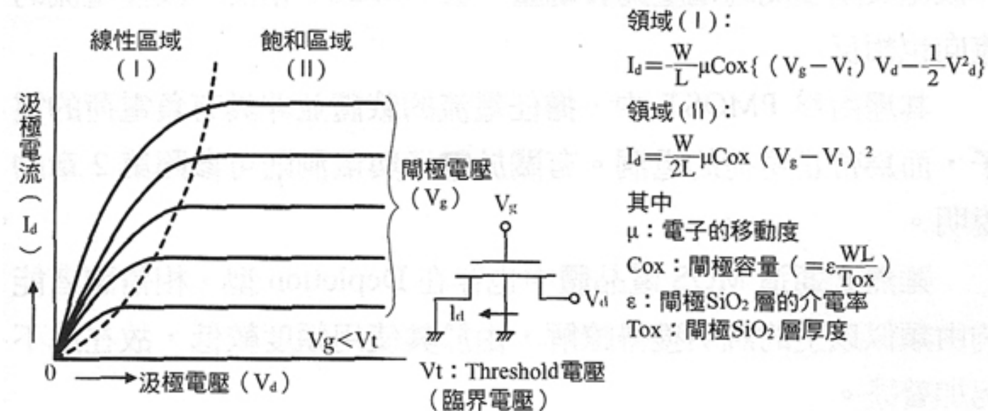
■圖 3 增強型P通道MOS電晶體的構造



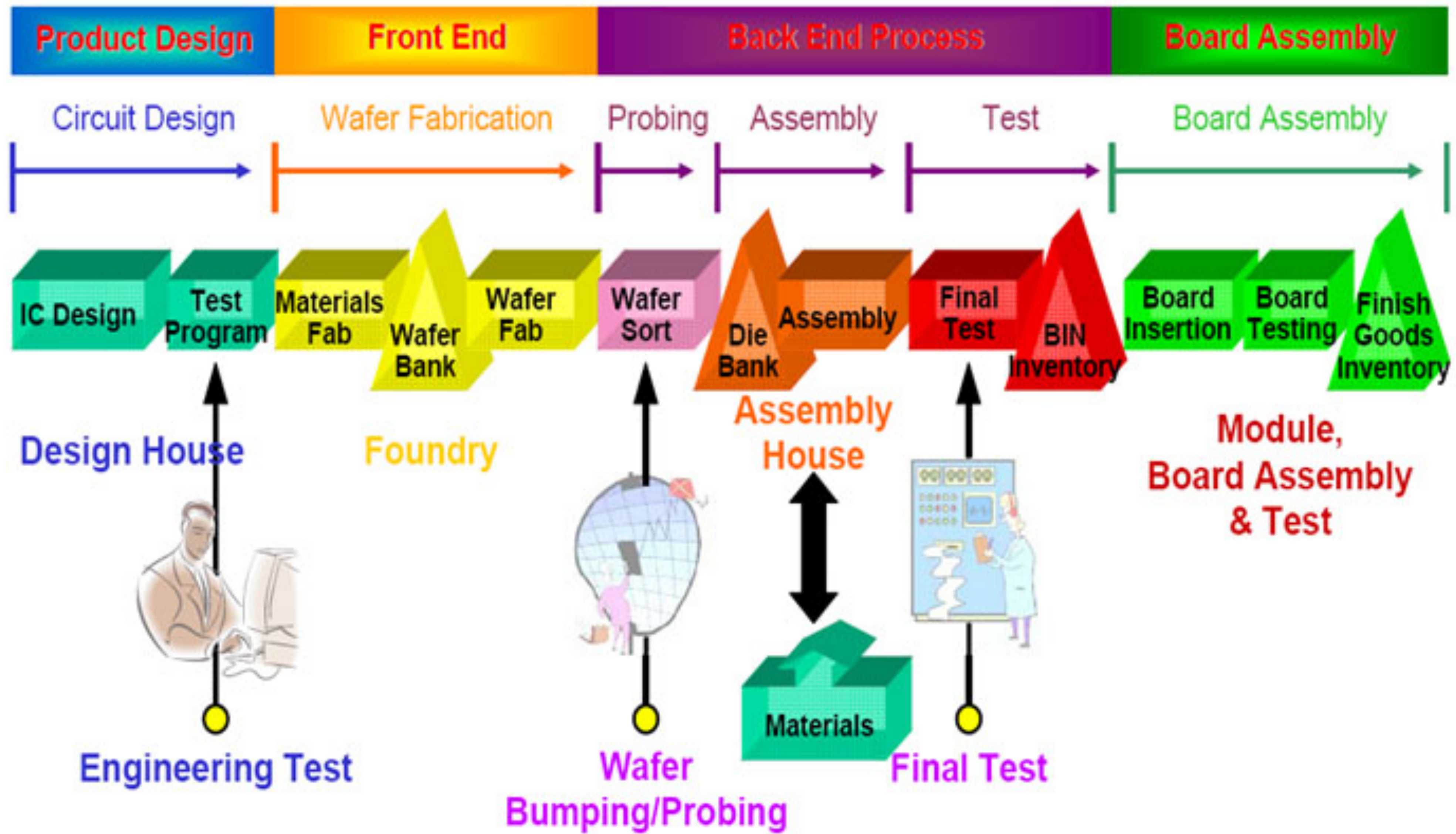
■圖 4 增強型P通道MOS電晶體的I－V特性



■圖 3 NMOST（E）的電流（I）－電壓（V）特性與特性式



Overview of semiconductor process - I



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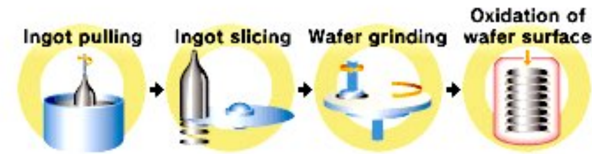
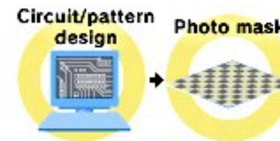
Overview of semiconductor process - II

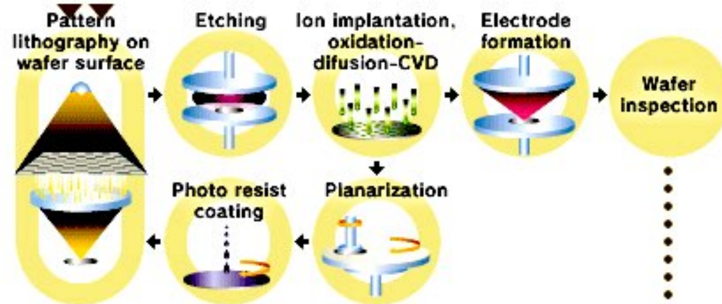
Wafer Fabrication Process



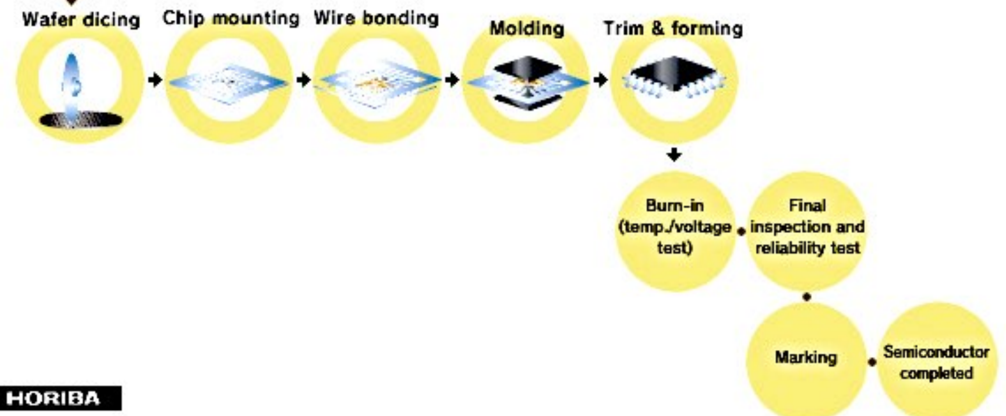
Mask Fabrication Process



Front-end Process



Back-end Process

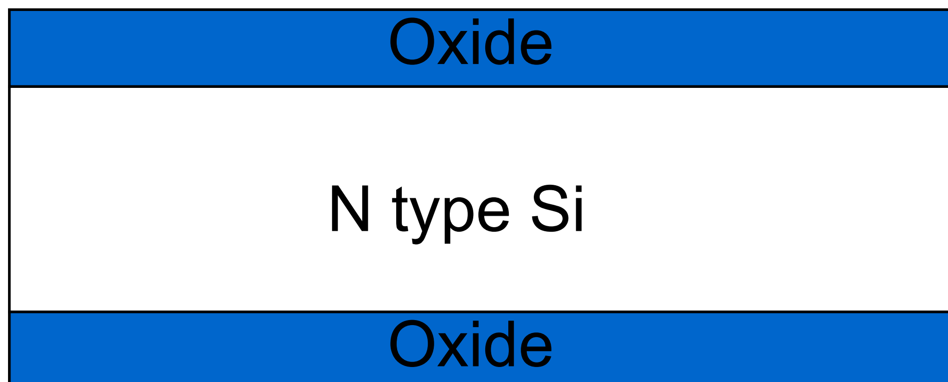


PMOS process

Oxidation

1. RCA clean

2. Wet Oxidation



- **What is RCA?**
- **Why do we need RCA?**
- **Thermal oxidation**
  - **Dry vs Wet**
  - **Thermally grown oxide vs Deposition oxide**
- **Oxide thickness**
  - **4000~5000 Å (400~500 nm)**

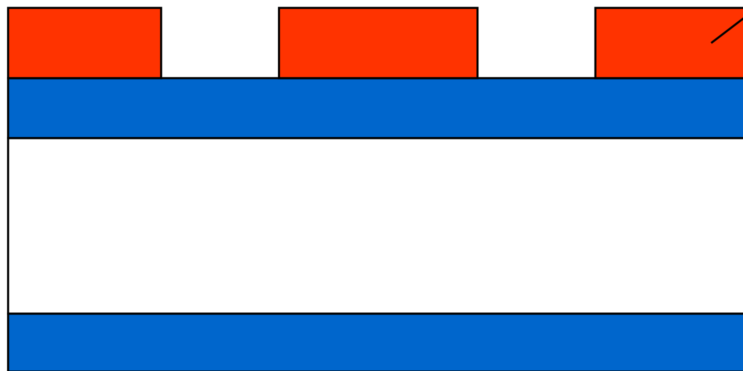
RCA clean

- Preliminary Cleaning (SPM)
  - Organic contamination is removed with a 5:1 H_2SO_4:H_2O_2 solution at 120℃.
- Standard clean-1 (SC-1)
  - Removal of insoluble organic contaminants/ particles with a 5:1:1 H_2O(DI water):H_2O_2:NH_4OH solution at 75℃.
  - Particles: Group IB, IIB, Au, Ag, Cu, Ni, Zn, Cd, Co, and Cr.
- Standard clean-2 (SC-2)
  - Removal of ionic and heavy metal atomic contaminants using a 75℃ solution of 6:1:1 H_2O:H_2O_2:HCl.
  - Metal: alkali ions and cations like Al^{+3}, Fe^{+3}, Mg^{+2}, (Au).
- Oxide strip
  - Removal of a thin silicon dioxide layer where metallic contaminants may accumulated as a result of cleaning, using a diluted 50:1/ 10:1 H_2O:HF solution.

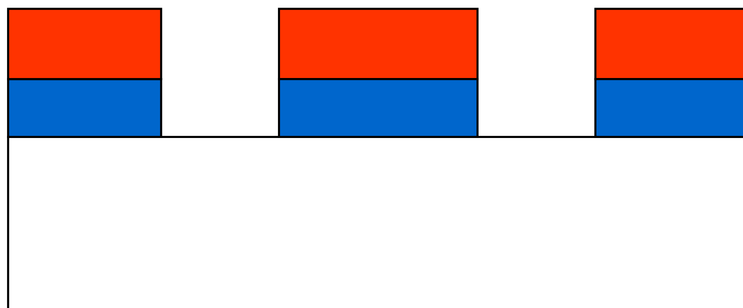
Lithography 1: Defining the source and drain

1. Litho-Mask #1

1 μm PR



2. (BOE) Wet Etching

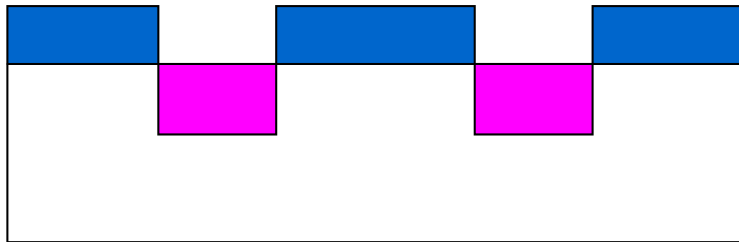


3. (H_2SO_4) PR Strip

- **Lithography process**
  - **Photoresist (PR) coating**
  - **Soft bake**
  - **Exposure**
  - **Development**
  - **Hard back**
- **Wet etching**
  - **BOE vs HF**
- **PR stripping**
  - **H_2SO_4 vs Stripper**

Dopant doping

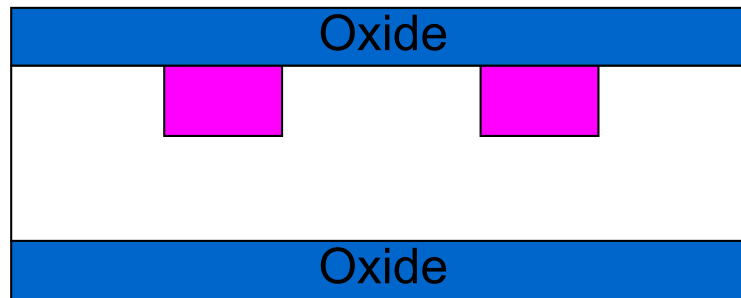
1. BOE dip
2. Diffusion



3. (BOE) Wet Etching

- Why dipping BOE first
- Dopant
  - N-dopant: Phosphor
  - P-dopant: Boron
- Ion implantation vs Thermal diffusion
  - Profile, cycle time…
- RTA (Rapidly thermal annealing) at 1000°C for 30s in Ar or N_2
  - Why RTA
  - Why no RTA for diffusion process
- Screen oxide removing

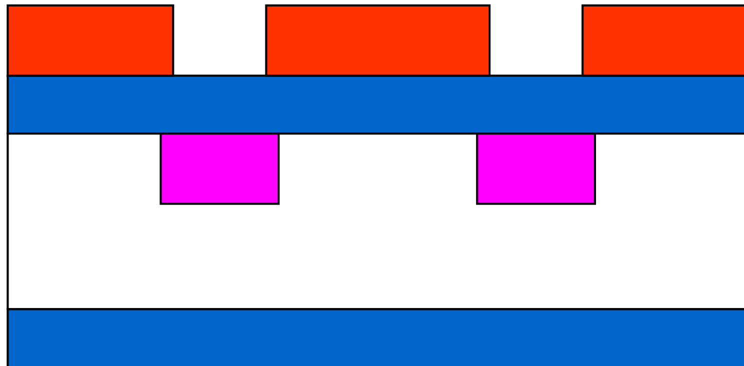
Gate oxide formation



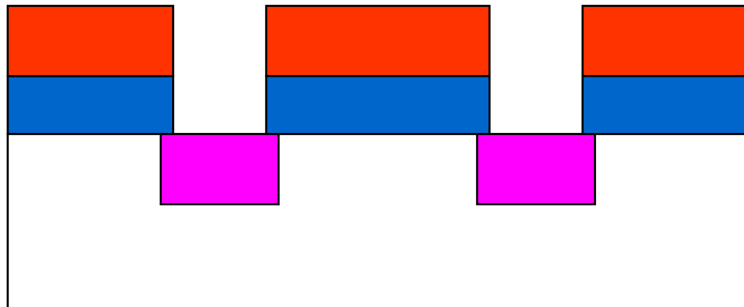
- Dry oxidation at 950°C to grow a oxide with 20-50 nm in thickness
  - Wet oxide vs Dry oxide
    - Last one is wet oxide, why don't we use wet oxide again?
  - Low temperature vs High temperature

Lithography 1: Defining the gate oxide

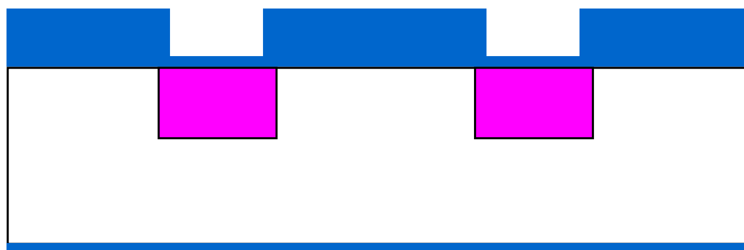
1. Litho-Mask #3



2. (BOE) Wet Etching



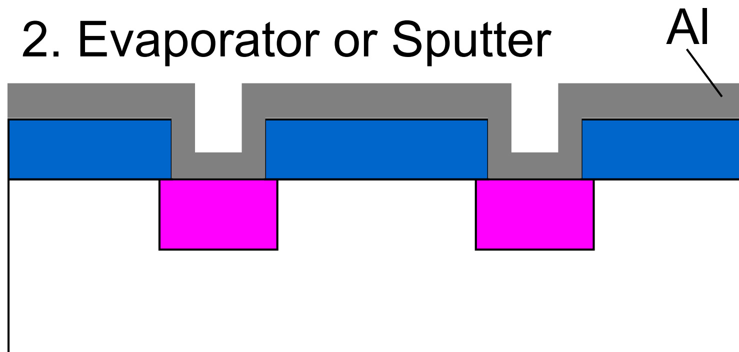
3. (H_2SO_4) PR Strip



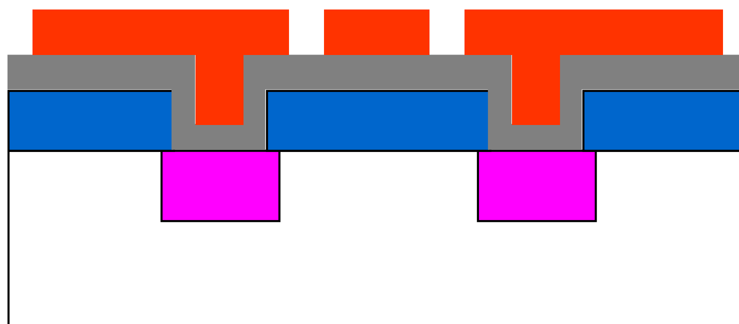
- What is alignment?
  - Size
  - Position
  - Type

Metallization

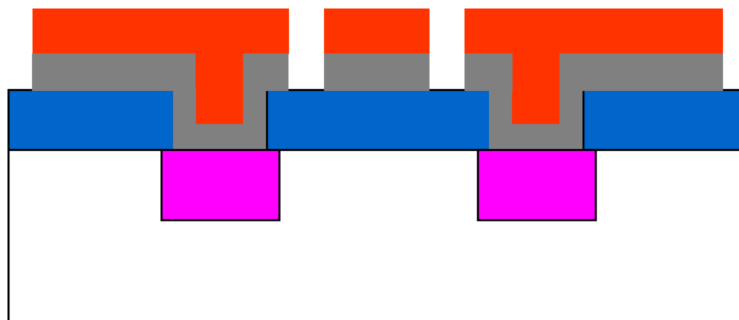
1. BOE dip
2. Evaporator or Sputter



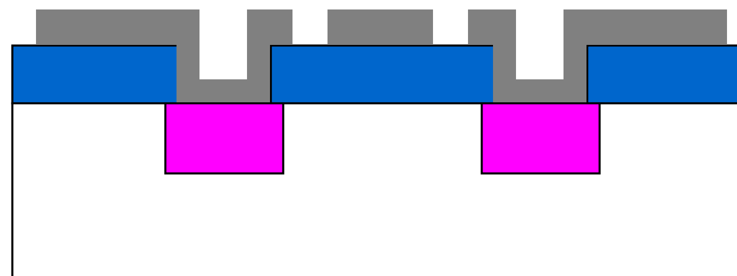
1. Litho-Mask #4



2. Dry Etching



3. (Acetone) PR Strip



- **400nm Al**
  - **E-gun evaporation vs Sputter**
- **Sulfuric acid vs Acetone**
- **Purpose of RTA**